# Electrical behavior of GaAs–AlAs heterostructures

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We report an experimental study of the electrical behavior of GaAs–AlAs–GaAs heterostructures grown by metal–organic chemical vapor deposition. The structures consisted of a layer of AlAs several thousand angstroms thick sandwiched between layers of GaAs which were a few microns thick. The top layer of GaAs was doped degenerately *n*-type with Se, while the bottom layer was nondegenerately doped. Capacitance–voltage (*C–V*) and curent–voltage (*I–V*) curves were obtained as a function of temperature, illumination, and rate of data acquisition. Deep-level transient spectroscopy (DLTS) measurements were also made. The *C–V* showed hysteresis near zero bias with the capacitance being larger when the voltage was swept from reverse to forward bias in the dark. The *C–V* displayed a light sensitive peak near zero bias. With illumination, the capacitance was greater, and no hysteresis was observed. We explain these phenomena as being due to deep levels near the AlAs–GaAs interface; DLTS has confirmed this. *I–V* curves taken in darkness also showed hysteresis. We take this as further evidence of deep levels. Additionally, capacitance failed to level off in reverse bias, indicating a lack of inversion in the samples.

## I. INTRODUCTION

Single barrier heterostructures are important constituents of many modern semiconductor devices. Structures as diverse as heterostructure transistors, quantum well lasers, and tunnel structures rely on the creation of barriers to electron transport.[1,2,3] These barriers are often realized by the epitaxial deposition of a wide band gap material in the midst of smaller band gap material, that is, with a heterostructure. The electronic properties of such constructions are thus of great importance.

We have studied GaAs–AlAs–GaAs heterostructures grown by metal–organic chemical vapor deposition (MOCVD). A variety of electrical measurement techniques were employed. These included capacitance–voltage (*C–V*), current–voltage (*I–V*), and deep level transient spectroscopy (DLTS) measurements. Our results may be summarized as follows. The *C–V* did not become constant in reverse bias, indicating a lack of inversion in the structure. The *C–V* also exhibited hysteresis near zero bias. The capacitance was larger when bias was swept from reverse to forward bias in the dark. With illumination the capacitance was larger, and no hysteresis was evident. These phenomena can be explained by the presence of deep electron traps near the AlAs–GaAs interface. DLTS measurements support this conclusion with direct evidence of these levels. *I–V* measurements show further evidence of deep levels, in that hysteresis was observed in these curves as well.

The samples we have studied can be generally classified as low current devices. This is because the barriers studied were fairly thick, and doping levels on the substrate side of the barrier were low. This was an advantage for the investigations reported here. In the case of *C–V* measurements, we were able to take *C–V* data over a large voltage range. In the case of *I–V* measurements, we were able to observe small effects, which might otherwise not be discernible. Finally, these samples were able to be examined with DLTS techniques. More conductive samples would have made this difficult.

## II. EXPERIMENTAL

The results reported here are due to the study of several samples of the same basic geometry. Structures were prepared by an MOCVD technique.[4,5] The samples consisted of a single AlAs barrier sandwiched between layers of GaAs. The top layer of GaAs (nearest the surface) was between 1 and 3 $\mu$ in thickness and was doped degenerately with Se at $1\text{–}3\times10^{18}$ cm$^{-3}$. The GaAs layer on the substrate side of the barrier and the AlAs barrier itself were lightly doped with Se in one case and not intentionally doped in all other cases. In these cases, the dopant was likely Se as well, as this was the dopant for the substrate. *C–V* profiles of this region indicated an *n*-type doping of between $7\times10^{15}$ and $3\times10^{16}$ cm$^{-3}$. This region was several microns thick. Doping levels in the AlAs are not known. This region ranged between 1000 and 4000 Å in thickness. The substrate was made up of GaAs doped degenerately with Si at roughly $3\times10^{18}$ cm$^{-3}$. A buffer layer of varying composition and thickness was grown on top of the substrate.

Photolithographic techniques were used to define Au–Ge contacts with diameters ranging from 70 to 450 $\mu$. Contacts were isolated from each other by wet etching using a 4:1:1 solution of $H_2SO_4$, $H_2O_2$, and $H_2O$. Ohmic contacts were made to the top and bottom of the samples by evaporation of an Au–Ge alloy and annealing for 20–30 s at about 400 °C. Prepared samples were then attached to TO-5 transistor headers, using conductive silver paint. Electrical connec-

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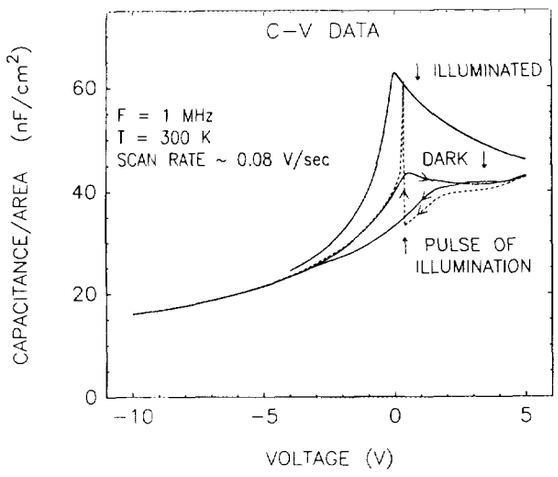


FIG. 1. Representative $C$–$V$ data. The direction of sweep is indicated by arrows. Note the hysteresis in curves taken without illumination. The curve of large capacitance was taken under illumination and is comprised of two curves, one for both bias sweep directions. The dotted curve was taken with a pulse of illumination at the point indicated by the arrow. All data are taken at room temperature.

tions to measurement circuitry were made, using gold wire probes or wire bonds.

$C$–$V$ and $I$–$V$ measurements were made, using Hewlett Packard equipment. An HP4192 LF impedance analyzer was used for $C$–$V$ measurements. An HP 4145 semiconductor parameter analyzer was used for $I$–$V$ measurements. An HP 9816 computer was used to control both instruments. The impedance analyzer was capable of monitoring the phase angle of the measured impedance. This phase angle was monitored during the data acquisition process. $C$–$V$ data presented in the figures were acquired digitally with a resolution of about 0.05 V and an effective sweep rate of about 0.083 V/s. $I$–$V$ data were acquired point by point as well with the parameter analyzer averaging a large number of measurements before recording a data point. Acquisition rates for the presented $I$–$V$ data were either 0.6 or 1.5 V/s. Rates were determined by independently measuring the time required to take a scan. Low temperature measurements were made, using an MMR Technologies refrigeration station. When data were taken under illumination, the illumination source was an incandescent lamp.

DLTS measurements were performed, using a method described by Lang.[6] An HP85 computer was used to control an MMR technologies refrigeration station. The computer was also used to acquire data from a double boxcar integrator, which sampled the capacitance output from a Boonton 72DB capacitance meter operating at 1 MHz. The method is similar to that employed by previous workers in this laboratory.[7]

We now describe general features of the data to be discussed. Reverse bias denotes negative voltage on the top layer of degenerately doped GaAs. Forward bias refers to positive voltage on the top layer. Capacitances are quoted in units of nanofarads per square centimeter. Currents are in picoamps. Finally, the AlAs–GaAs interface refers to the interface between the AlAs and the low doped GaAs layer.

## III. RESULTS

### A. Capacitance results

In Fig. 1, we present data representative of the $C$–$V$ behavior of all the samples represented in this article. Some of these results have been presented previously.[8] Initially, one observes that the capacitance does not level out in reverse bias. This implies that the depletion region is continuing to expand. This continues to occur to the breakdown voltage of the device, which was usually about 25 V, but was as large as 50 V in one case. One can conclude from this that no inversion takes place in this structure. This is explained as being due to poor confinement of minority carriers by the AlAs valence band.[9]

Near zero bias, hysteresis is evident in $C$–$V$ curves taken without illumination. When voltage is swept from forward to reverse bias, the capacitance is observed to be lower than when bias is swept the other way. This indicates a nonequilibrium process. This behavior can be explained by the presence of electron trap levels spatially localized near the AlAs–GaAs interface. Empty traps, being positively charged, contribute to the voltage in the depletion region, whereas filled traps do not. The capacitance at zero bias will be different, depending upon the initial charge state of the deep levels. The absence of such hysteresis has been used as evidence for the lack of deep levels in similar structures.[10]

Consider first the case in which bias is swept from reverse to forward bias in the dark. In this case, electron traps in the depletion region will be empty. There will not be a significant number of electrons near the trap levels until the depletion edge, which is a few extrinsic Debye lengths wide,[11] nears the trap levels. They then begin to fill, thus necessitating additional depletion of free carriers and a consequent decrease in capacitance. This decrease stops when the trap levels return to equilibrium with applied bias.

The levels are initially filled when voltage is swept from forward to reverse bias. When the depletion region sweeps over the trap levels, they begin to empty. This process is, in the absence of illumination, a thermal one. When voltage is swept fast enough, the population of filled levels is not in equilibrium with the applied bias. Some levels that were empty when voltage was swept the other way are now filled, thus requiring additional free carrier depletion and a lower capacitance. The two curves meet when the number of empty levels increases to an equilibrium level. When data are taken very slowly, both the hysteresis and the peak in the capacitance are no longer evident.[8]

In Fig. 1, we also present data taken under illumination. In this case, there is no hysteresis. This is because light provides a nonthermal means to empty the trap levels. Overall capacitance is greater, because charge in the depletion layer is increased by the light. A peak in the capacitance continues to be observed. This is because the number of electrons near the traps continues to change as the depletion width sweeps across the spatial position of the levels.

One further $C$–$V$ curve is presented in Fig. 1. Voltage was swept from forward to reverse bias in this curve. At the start of the curve, trap levels are filled and the $C$–$V$ curve is parallel to the reverse going curve. At about 0.3 V, the sample was

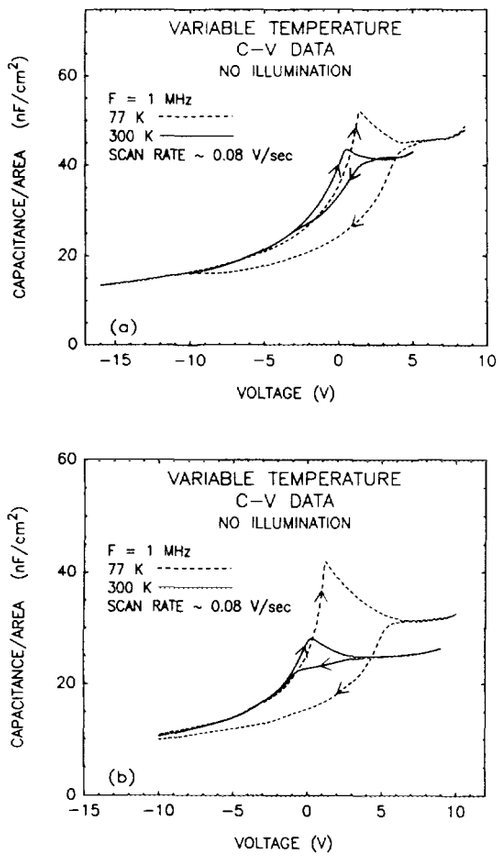


FIG. 2. $C$–$V$ curves for two samples at 300 and 77 K. Note the increase in hysteresis for 77 K curve and the shift of the peak to more forward bias. The direction of sweep is indicated by arrows.

briefly exposed to illumination. Trap levels are emptied, and photoexcited carriers are created. The capacitance, therefore, rises to its illuminated value. The illumination ceases, and the capacitance decays, due to the relaxation of photoexcited carriers. In the illustrated case, the depletion edge has already crossed the position of the trap levels. This means that the traps remain empty. Therefore, the capacitance relaxes to values associated with the *forward* going curve. This experiment serves to verify the explanation presented for the $C$–$V$ behavior of the samples. It links all three curves together, reverse going, illuminated, and forward going.

For one sample, the hysteresis effect was investigated as a function of frequency at room temperature in the dark. The hysteresis effect was seen to remain almost constant for ac oscillator frequencies ranging from 10 kHz to 5 MHz. In fact, the entire $C$–$V$ curve was changed very little by varying the measurement frequency. This can be taken to mean that the emission rate of the traps is far below this frequency range.

In Fig. 2, we present $C$–$V$ data for two samples at 300 and 77 K. The hysteresis described previously increases as temperature decreases. Additionally, the peak in the forward going curve shifts to more positive voltage and is more pronounced. This can be explained by the longer emission time of the deep levels and the more sharply defined depletion edge, both of which are obtained at lower temperatures.

One can gain some insight into the nature of the deep levels from the data presented in Fig. 2. Initially, one observes that they must be electron traps, since they are positively charged when empty. Also, one observes that their emission time should be quite long. Rough estimates would indicate several seconds at room temperature. A rough concentration estimate can be made from the difference in capacitance between forward and reverse going curves. The total capacitance is the series combination of the AlAs and the GaAs depletion layer capacitances. At the bias at which the forward going curve is peaked, we have

$$\frac{1}{C_1} = \frac{1}{C_i} + \frac{w_1}{\epsilon_s},$$

where $C_1$ is the capacitance of the forward going curve at this point, $C_i$ is the saturation capacitance of the AlAs in forward bias, $w_1$ is the depletion width, and $\epsilon_s$ is the dielectric constant of GaAs. Similarly, for the reverse going curve, at the same bias,

$$\frac{1}{C_2} = \frac{1}{C_i} + \frac{w_2}{\epsilon_s}.$$

Solving for the difference in depletion width $\delta w = w_2 - w_1$:

$$\delta w = \frac{(\delta C)\epsilon_s}{C_1 C_2},$$

where $\delta C = C_1 - C_2$. We equate the carrier density, $N_d(\delta w)$, contained in this region to the deep level sheet concentration:

$$N_d(\delta w) = N_t.$$

This estimate yields concentrations in the $10^{11}$ cm$^{-2}$ range for both samples in Fig. 2 at 77 K. Concentration estimates are somewhat lower (less than an order of magnitude) when made at 300 K. This is due to the longer trap emission time obtained at low temperature.

In Fig. 2, the saturation capacitance is observed to change as temperature changes. In forward bias, conventional theory[12] dictates that the capacitance should level off at approximately

$$C = C_i = \frac{\epsilon_i}{d},$$

where $\epsilon_i$ is the dielectric constant of AlAs, and $d$ is the thickness of the AlAs. Barrier thickness for the sample in Fig. 2(b) was measured with a scanning electron microscope (SEM) to be about 2500 Å. The thickness prediction at 77 K is about 2800 Å. At 300 K, the thickness prediction is about 3600 Å. The decrease in predicted thickness between 300 and 77 K is suggestive of negative charge in the barrier. That is, the AlAs is slightly $p$ type. Ionized acceptors could deplete parts of the GaAs, thus resulting in a lower saturation capacitance than that of the AlAs alone. As temperature goes down, the number of ionized acceptors decreases, thus decreasing the amount of depletion and raising the saturation capacitance. Donor density for the sample in Fig. 2(a) is larger than that for Fig. 2(b). This is consistent with the observation that Fig. 2(a) does not show as much change in saturation capacitance as Fig. 2(b). It further suggests that

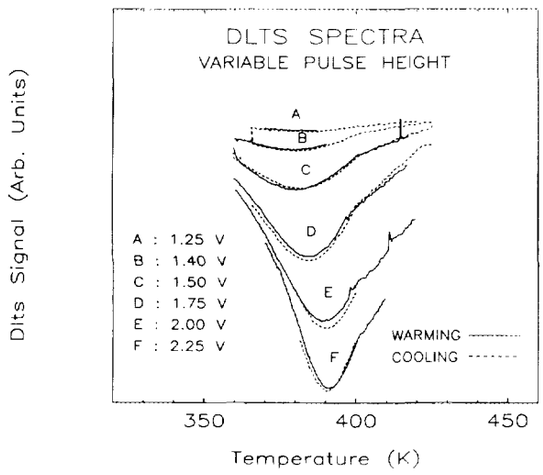


FIG. 3. DLTS curves for a variety of labeled pulse heights. Quiescent reverse bias, pulse width, and rate windows are held constant. Warming and cooling spectra are both presented. Quiescent reverse bias is $-1.0$ V. Note the peak shift.

acceptor density may be larger for the sample of Fig. 2(b).

When a sample with a barrier doped heavily with Mg was studied, the discrepancy between predicted and SEM measured barrier thickness was quite large. Room temperature $C$–$V$ predicted about 4000 Å, whereas the SEM showed the barrier thickness to be about 1000 Å. A rough calculation, treating the junction between the AlAs, doped at $1\times10^{18}$ $cm^{-3}$, and the GaAs, doped at $1\times10^{16}$ $cm^{-3}$, as a simple $p^+n$ junction, yields sufficient depletion to achieve the observed result.[12]

Finally, one sample was studied in which the barrier was intentionally doped $n$ type, while all other sample parameters remained unchanged. This sample showed much higher levels of conduction than those reported here. One can generalize these results to conclude that all the samples reported on here had barriers which were more or less $p$ type. This sort of general information about the barrier itself is valuable, because barrier composition information is difficult to obtain. More generally, these results suggest that band bending is a very important factor in determining the conductivity behavior of barrier structures.

## B. DLTS results

DLTS studies were performed on two samples. The basic results of the DLTS measurements corroborate and expand the observations of the $C$–$V$ studies. Only general information will be taken from the data presented. Electron trap levels were observed. These levels were observed to be localized near the interface with possible extension into the AlAs. Evidence for interface state presence or multiple spatially localized deep levels was observed. Activation energy plots were made for both samples, which suggest that the same level was seen in both cases.

In Fig. 3, we present a series of DLTS spectra of one sample. The variable parameter in these scans was the magnitude of the pulse. The pulse duration, quiescent reverse bias, and rate windows were not changed. One observes that the size of the DLTS peak increases as the pulse height increases. Further, the peak of the spectra increases with the pulse height. No trap signature was observed for pulse heights below 1.0 V at a quiescent reverse bias of 1.0 V. Indeed, the trap signature at this level was extremely small. This bias corresponds to a depth of about 1500 Å from the barrier. This means that the trap levels extend less than this distance into the GaAs. As the quiescent bias level was brought into forward bias, the trap signature decreased. This indicates that the deep levels are isolated near the AlAs–GaAs interface. However, the extent to which the AlAs was scanned is not known. Therefore, it is not possible to say how far into the AlAs these levels extend.

The significance of the observed peak shift is as follows. For a conventional metal–insulator semiconductor (MIS) structure, increasing pulse height allows additional regions of the interface to be scanned. If interface states are present in the energy gap, additional states will be able to participate in the DLTS emission process as the pulse height increases. This will change the shape of the DLTS capacitance transient and the peak of the DLTS spectrum shifts. Therefore, observation of peak shift in a series of DLTS spectra of an MIS structure is indicative of interface states.[13] The structures we have studied are not pure MIS structures. Therefore, one cannot say conclusively that the observed peak shift indicates their presence. The shift could be due to other things as well. More than one bulk level could produce the effect. Both bulk levels and interface states may be present; this is often the case.[14,15] Factors, such as interdiffusion at the AlAs–GaAs interface, could also be important.

Using a standard method,[6,14,15] trap concentration can be obtained. This method, which relates trap concentration to the variation of the DLTS peak with pulse height, is not accurate for deep level concentrations approaching that of the shallow level. $C$–$V$ analysis has shown that the trap level concentration could be this large. Thus, the rough estimate of trap concentration of $1\times10^{15}$ $cm^{-3}$ one gets from this method is probably below the actual concentration.

In Fig. 4, activation energy plots for the deep levels observed, corrected for the $T^2$ exponential prefactor, are presented. These plots are informative, even though the peak in the DLTS spectra represented by each point of the plot is subject to the peak shift phenomena described above. First, the possible peak shift is not very large. Second, the data from the two samples are very similar. This suggests that the same level is being observed in *all* samples.

Figure 4(a) yields an activation energy of 500 meV with a standard error of 70 meV and a capture cross section of $6\times10^{-18}$ $cm^{-2}$. Figure 4(b) also yields an activation energy of 500 meV with a standard error of 40 meV and a capture cross section of $1\times10^{-17}$ $cm^{-2}$. Owing to the limited range of emission rates obtained, the capture cross section data are not very accurate. These data yield emission times of several seconds. This is in good agreement with capacitance data.

## C. Current–voltage results

$I$–$V$ measurements were made on all samples. Measurements were made with and without illumination. When not illuminated, the currents typically observed were below a

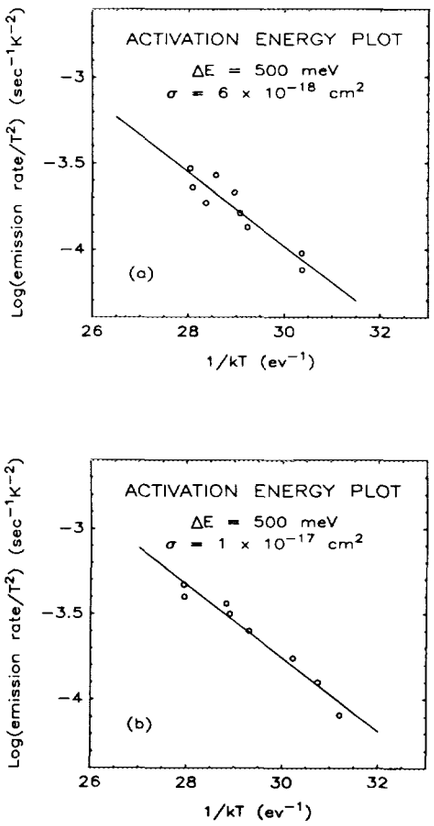


FIG. 4. $T^2$ corrected activation energy plots for two samples. $\Delta E$ is the activation energy. Standard error in $\Delta E$ is 70 meV for (a), and 40 meV for (b). $\sigma$ is the capture cross section. Both samples show the same activation energy. This implies that the same trap is present in both samples.

nanoamp. Hysteresis was observed in the $I$–$V$ curves of all samples studied. This hysteresis was investigated as a function of rate, temperature, and illumination. When illuminated, currents are much larger, and no hysteresis is observed.

In Fig. 5, we present a representative $I$–$V$ curve. No light falls on the sample in the pictured voltage range. Consider the curve obtained by sweeping voltage from negative to positive values. With the sample in reverse bias, it was briefly exposed to light. As voltage becomes positive, a sudden increase in current is observed. This increased current is maintained at an almost constant level until large scale conduction begins. This is not observed when the $I$–$V$ curve is taken with bias swept from forward to reverse values.

This result can be explained by the same deep levels whose presence was evidenced by $C$–$V$ and DLTS studies. If the sample is illuminated in reverse bias, trap levels are emptied. This pulse of light serves to provide a known initial state for the trap levels, making analysis simpler. As voltage is swept toward forward bias, some levels will fill, but most will remain empty. As the depletion edge crosses the spatial position of these empty levels, they begin to fill. As they fill, the number of electrons in the measuring circuit decreases. This time rate of change of carriers is the current enhancement observed.

When the data are taken starting from forward bias, the aforementioned deep levels are filled at the outset. As the depletion region envelopes the deep levels, they begin to thermally empty. This process does not produce a sudden increase in the number of carriers. Therefore, no jump in current is observed when data are taken this way.

An estimate of the number of deep levels required to create this effect can be made. The area under the enhanced current part of the $I$–$V$ curve can be approximated as a rectangle. The area of this rectangle can be converted to a charge, and, hence, to a sheet concentration as

$$N_t = \frac{I_s(\delta V)}{ARq},$$

where $I_s$ is the height of the current step, $\delta V$ the voltage range over which the enhanced current persists, $A$ is the area of the device, $R$ is the rate at which voltage is changed, and $q$ is the electronic charge. The devices pictured in Figs. 5 and 6 were 350 $\mu$ in diameter. Taking 40 pA as the size of the current step in Fig. 5, and 2 V as the voltage range, we obtain a concentration of about $3\times10^{11}$ cm$^{-2}$. This agrees well with the estimates of concentration made from $C$–$V$ data.

In Fig. 6, we present variable temperature $I$–$V$ curves for one sample. Two different rates are presented. The faster rate, in Fig 6(b), is obtained with less averaging by the parameter analyzer and is thus noisier. These data show how the hysteresis effect varies with temperature. The data were obtained by illuminating the sample briefly, during reverse bias. The spatial location and energetic position in the gap of the levels will both play a role in determining the voltage at which the enhanced current begins. This onset voltage is very sensitive to the point at which illumination was applied in reverse bias. The reason for this is that the time at which the sample was last illuminated will influence both the number and the location of empty levels available to participate in the effect. The variation in the onset voltage shown in Fig. 2 is due to this effect. No systematic variation with temperature of this onset voltage was observed.

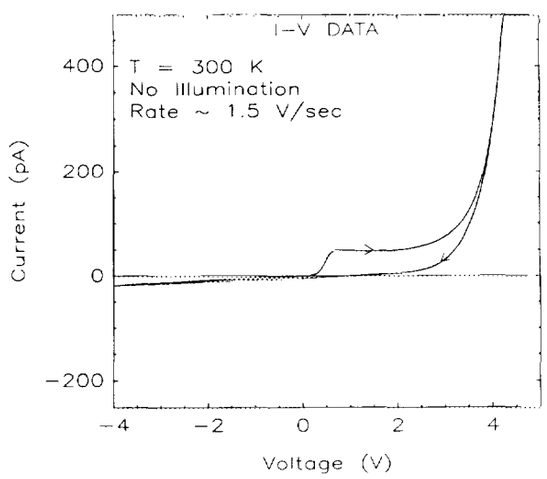


FIG. 5. $I$–$V$ curves for one sample at room temperature. Direction of sweep is indicated by arrows. In the forward going sweep, trap levels were emptied at about $-5$ V by brief exposure to illumination. The hysteresis is due to trap filling effects.

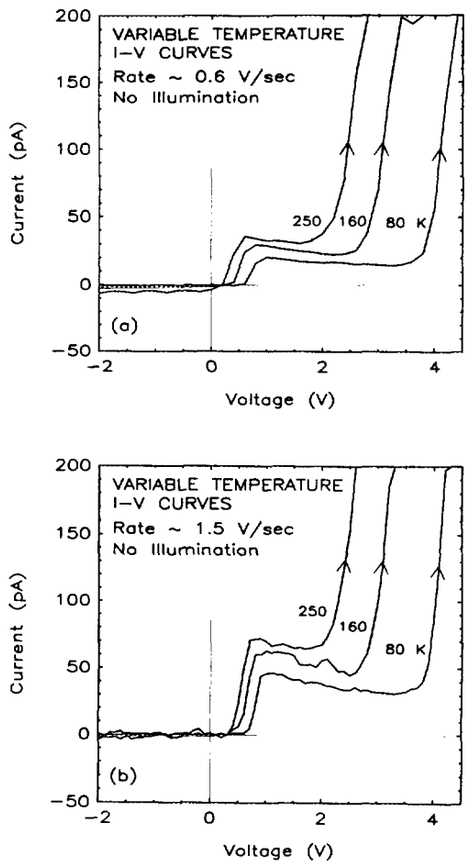


FIG. 6. Variable temperature $I$–$V$ curves for the same sample at different rates. Note the increase in size of current jump as rate increases. Note also the decrease in current jump with temperature, at a given rate. To empty levels, devices were exposed to brief illumination at a bias of about $-4$ V. Greater noise is observed in (b) because of decreased data averaging.

It is seen in Fig. 6 that the height of the current step decreases as temperature decreases. This can be explained by the general decrease in current as temperature goes down. There are fewer electrons passing over the trap levels, and, thus, the number which drop into traps to supply additional current is smaller as well. Also, one observes that the onset of large scale conduction of the device advances to more positive voltages as temperature goes down. Thus, the voltage range over which hysteresis is observed is seen to increase. These two effects combine to keep the trap concentration estimate (as calculated above) roughly constant in the $10^{11}$ $cm^{-2}$ range.

As the acquisition rate increases, the current jump becomes larger. This can be seen by comparing Fig. 6(a) to Fig. 6(b). This is because a faster sweep rate allows a more rapid change in the carrier population. This increased rate of change in the number of carriers results in a larger current jump. Conversely, the current jump goes to zero as the rate decreases to very slow values. Since the same number of traps are being filled in each case, the trap concentration estimate, obtained as above, is about the same for Figs. 6(a) and 6(b).

## IV. CONCLUSIONS

We have studied the behavior of MOCVD grown GaAs–AlAs–GaAs heterostructures, using $C$–$V$, DLTS, and $I$–$V$ measurements. These three methods combine to provide some information about the samples studied. They are low current structures, having a slightly $p$-type barrier; they do not exhibit inversion. The samples exhibit light sensitivity in both the $C$–$V$ and the $I$–$V$. There are deep electron trap levels associated with the AlAs–GaAs interface with less than 1500 Å extension into the GaAs and possible extension into the AlAs. The sheet concentration of these levels is in the low $10^{11}$ $cm^{-2}$ range.

Results of this study can have significant impact on MOCVD grown devices, using structures of this type. The observed lack of inversion poses problems for $p$-channel field effect transistors. High electron mobility transistors (HEMT's) and any other device relying upon conduction alongside the barrier of a structure of this type will suffer efficiency losses due to the observed trap levels. The observed hysteresis is an interesting memory effect, which could be an important consideration in the behavior of low current devices.

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